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Enhancement of Efficiency of a Solar Cell Fabricated on Black Si Made by Inductively Coupled Plasma–Reactive Ion Etching Process: A Case Study of a n-CdS/p-Si Heterojunction Cell

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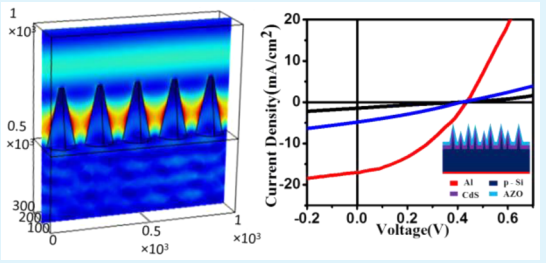
ABSTRACT: We show that a significant enhancement of solar cell efficiency can be achieved in cells fabricated on black Si made using inductively coupled plasma–reactive ion etching (ICP-RIE). The ICP-RIE-fabricated black Si results in an array of vertically oriented defect-free Si nanocones (average height ∼150 nm; apex diameter ∼25 nm) exhibiting an average reflectance ≤2% over most of the relevant solar spectral range. The enabling role of the ultralow reflectance of the nanostructured black Si has been demonstrated using a heterojunction solar cell fabricated by depositing a n-type CdS film on p-Si nanocones followed by a transparent conducting coating of Al-doped ZnO (AZO).



The fabricated n-CdS/p-Si heterojunction exhibits promising power conversion efficiency close to 3%, up from a mere efficient 0.15% for a similar cell fabricated on a planar Si. The effect of the fabrication process for the black Si on solar cell performance has been investigated through the measurements of carrier lifetime and surface recombination velocity. The accompanying model and simulation analysis shows that the conical structure leads to the effective dielectric constant varying smoothly from the value of the air at the top to the value of Si at the base over the length of the nanocone, leading to a substantial reduction of its reflectance.

KEYWORDS: *black Si, inductively coupled plasma–reactive ion etching, radial heterojunction, CdS/Si heterojunction, surface recombination velocity*

1. INTRODUCTION

Vertical nanostructure arrays on Si surfaces, such as nanowires, nanocones, nanopillars, nanotubes, and nanoholes, have attracted considerable research interest because of their remarkable physical properties due to the combined effect of confined dimensions and high surface-to-volume ratio in comparison to those of bulk. They can be used as templates for fabrication of radial heterojunction, attractive for optoelectronic applications.[1−3] In particular, surface-modified silicon, having micronanostructures on the top, exhibits extremely low reflectance (∼2%) and is known as "black Si" (BSi). Because of its beneficial fundamental properties, BSi has been explored for various practical applications such as solar cells,[4−6] light-emitting devices,[7,8] antibacterial coatings,[9] energy storage,[10] and gas sensors.[11,12] Because of its excellent antireflection property, BSi is under critical examination for solar cell application and represents a very active research area in the field of renewable energy. Extensive research has been done to fabricate BSi by creating various vertical nanostructures on a silicon surface by different approaches, such as reactive ion etching,[13,14] femtosecond laser-pulse irradiation,[15] metal-assisted wet etching,[16,17] and electrochemical etching,[18] and to explore fabrication of nanowire heterojunction-based optoelectronic devices. In recent years, solution-based chemical techniques have been proposed as cost-effective alternatives.[19] The proposed processing, however, is limited to single-crystalline silicon (c-Si) only and is not very effective in multicrystalline silicon (mc-Si) because of the different orientations of grains. The presence of rough surfaces in chemically grown Si nanostructure is another concern because a defect-free interface is highly desirable for efficient heterojunction devices.

Plasma processing to make BSi is an attractive alternative. In the present work, we have fabricated highly antireflecting Si nanostructures (reflectance ≤2%) over a spectral range of 350–1000 nm with a high-quality defect-free surface using a one-step inductively coupled plasma–reactive ion etching (ICP-RIE) technique. ICP-RIE is a plasma-based technique that is the preferred route for anisotropic etching with vertical profiles, higher etch rates, and essentially low surface damage. Low surface damage is highly desirable for fabrication of heterojunction solar cell devices. The ICP-RIE process is compatible with current processing techniques for a number of different types of solar-cell fabrication tools.

On the other hand, the heterojunction of nanotextured Si with a group III–V or II–VI semiconductor has attracted much

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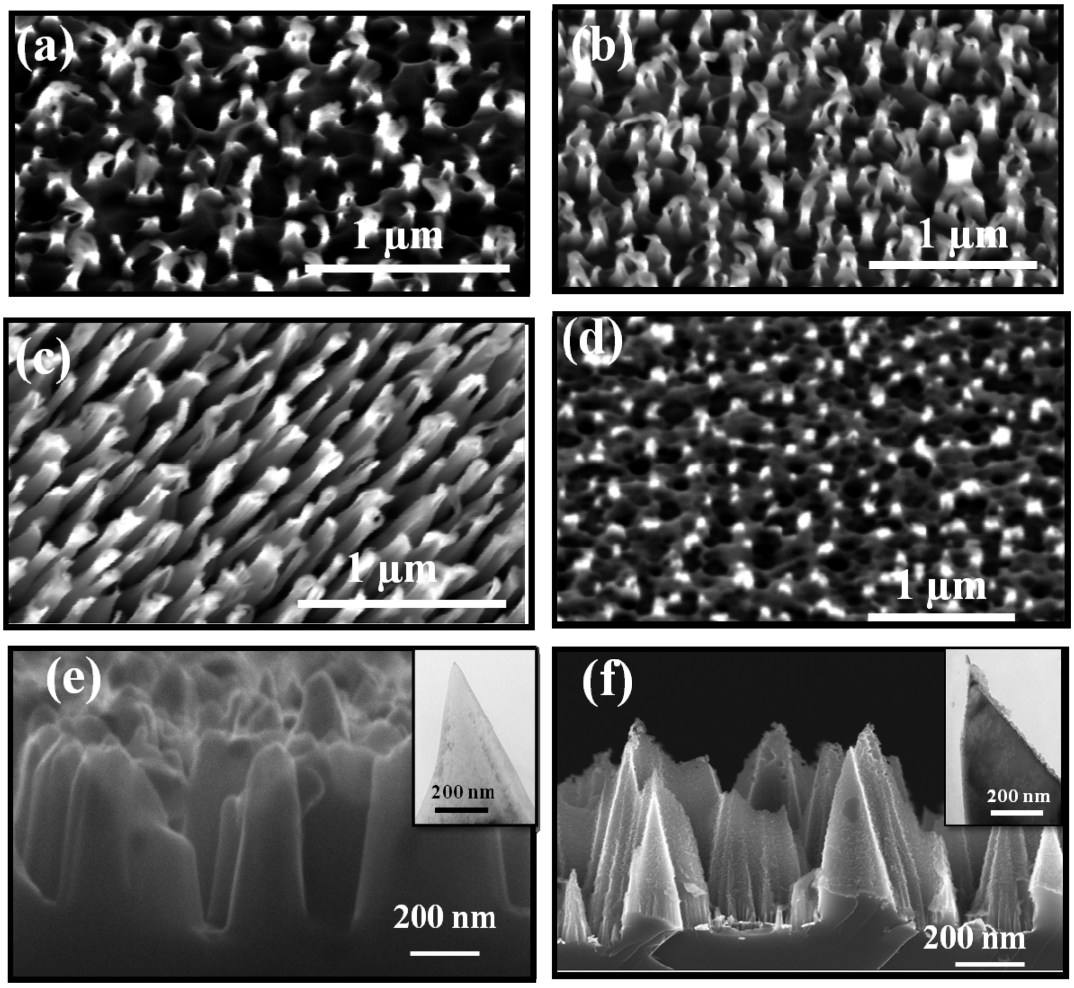

Figure 1. FESEM images of Si nanostructures fabricated through ICP-RIE technique at different ICP powers (a) 100 W, (b) 125 W, (c) 150 W, and (d) 200 W. (e) Magnified image of Si nanostructure fabricated at ICP power of 150 W. (f) Si nanostructures fabricated through MACE technique. Insets of the e and f show typical TEM images of Si nanocones fabricated with ICP-RIE and MACE techniques, respectively.

attention in developing efficient solar cells in the past several years.[20] CdS is an important n-type, direct band gap, group II−VI semiconductor with strong optical absorption in the visible range. There are some studies on fabrication of n-CdS/p-Si heterojunctions for optoelectronic devices. Hayden et al. reported radial heterostructures using p-type silicon and n-type CdS nanowires for application as a light-emitting device,[21] Manna et al. fabricated a highly efficient n-CdS/p-Si radial nanowire heterojunction photodetector on chemically etched Si nanowire templates.[22] Few research groups have also explored n-CdS/p-Si heterojunction for solar cell application,[23−25] but most of the reports are based on Si/CdS heterojunction fabricated on planar Si. The above studies indicates that Si/CdS heterojunction for solar cell application needs more investigation and that a heterojunction on highly antireflecting BSi might be a promising candidate for the assembly of high-efficiency solar cells.

To establish the enabling role of such a plasma-processed Si nanostructure BSi for enhancing solar cell efficiency, we fabricated a radial heterojunction with a thin film of n-CdS deposited on the p-type Si nanostructure. The efficiency achieved (under 1.5 AM condition) is ∼3%, which is substantially larger than the 0.15% efficiency achieved with planar Si. Though the enabling role of the plasma-processed BSi is demonstrated only on a n-CdS/p-Si heterojunction cell, it is a generic value-addition process that can be used to enhance the efficiency of different types of Si-based solar cells.

2. EXPERIMENTAL SECTION

Vertically aligned Si nanostructure arrays (SiNs) on boron-doped p-type single-side-polished Si(100) substrates (resistivity = 2−10 Ω cm) were fabricated by ICP-RIE etching technique using silver nanoparticles as a mask. Si substrates were first cleaned through the standard RCA cleaning process. Thereafter, a uniform layer of Ag nanoparticles (Ag NPs) on cleaned Si were prepared by depositing a Ag film ∼10 nm thick by thermal evaporation, followed by annealing in an inert atmosphere at 400 °C for 1 h. Si pieces of 2 × 2 cm^2 in size coated with Ag NPs (average diameter of ∼50 nm) were then transferred into the SENTECH SI 500 ICP-RIE system employing CF_4 gas to etch the unmasked area. In CF_4-based plasma etching system, under application of an electric field, free electrons collide with neutral molecules of CF_4, resulting in dissociation of CF_4 into electrons, ions, and fluorine radicals because of dissociative ionization, resulting in the formation of volatile SiF_4. Though dry etching is a combination of both physical and chemical mechanisms, outer Si atoms are dominantly removed by chemical reaction in an ICP-RIE process. Although the ICP power controls the plasma density, an additional RF source is coupled capacitively to the substrate holder to adjust the substrate bias voltage. The bias voltage to the substrate is generally very low, on the order of a few tens of volts only, offering low velocity with which ions hit the substrate. As a result, the ICP-RIE method provides minimal ion-induced damage. Substrate temperature,

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gas flow rate, and chamber pressure were kept at constant values of 20 °C, 0.6 Pa, and 40 sccm, respectively, which are found to be optimal for growth. ICP and RF powers were varied to attain the desired aspect ratio for lowest reflectance in Si nanostructures.

To fabricate n-CdS/p-Si heterojunctions on ICP-etched Si nanostructures, CdS film was deposited by a pulsed-laser deposition (PLD) technique from a high-purity (99.999%) CdS target. The residual Ag from ICP-etched nanostructures was removed by putting the templates in concentrated nitric acid for 15 min prior to CdS deposition. The removal of Ag has been confirmed by using EDAX after the acid treatment. All samples were treated with 2% HF to remove native oxide from Si surfaces just before the deposition. Si nanostructure templates were placed at a distance of 10 cm from the CdS target. The target was ablated using a KrF excimer laser (λ = 248 nm) at an energy density of ~2 J/cm^2 with the repetition rate of 5 Hz to deposit a CdS film around 100 nm thick on Si nanostructures. During deposition, the temperature of the substrate was maintained at 300 °C, and the typical pressure inside the chamber was ~10^{-7} Torr. To complete the device fabrication, nearly 20 nm of transparent and conducting Al-doped ZnO (AZO) film was deposited by PLD in the same chamber. A thick aluminum layer was deposited by thermal evaporation onto the backside of the devices to form the bottom ohmic contact. To establish the superiority of the plasma-processed BSi compared to chemically processed BSi, we made a similar solar cell on nanostructured Si made by metal-assisted chemical etching (MACE). The fabrication process of BSi via the chemical route has been discussed in detail in our previous study.[19] As a reference, a solar cell with planar c-Si is also made on a Si(100) wafer.

Surface morphology of Si and CdS/Si nanostructures was studied by field-emission scanning electron microscopy (FESEM). Photoluminescence measurement was carried out using a monochromator and photomultiplier detector in the range 400−800 nm using a He−Cd laser as the excitation source operating at 325 nm with an output power of 40 mW. The current−voltage (I−V) characteristics of the heterojunctions were studied using a Keithley 4200-SCS measurement unit along with a solar simulator under AM 1.5 (100 mW/cm^2) solar irradiation conditions. External quantum efficiency (EQE) was measured using quantum efficiency/IPCE measurement system equipped with lock-in amplifier, monochromator, and broad-band light source. The recombination-limited minority carrier lifetime was measured using open-circuit photovoltage (V_{oc}) decay technique. V_{oc} decay profiles were recorded at the trailing edge of 980 nm diode laser source pulse (model no. Newport LQD980-220E), with an illuminated power of 28 mW cm^{-2} at room temperature. The transient responses were recorded using internal oscilloscope of Keithley 4200-SCS measurement unit.

3. RESULTS AND DISCUSSION

3.1. Fabrication of Si Nanocones with Very Low Reflectance Using ICP-RIE. To produce vertically aligned Si nanostructures by the top-down approach, Si wafers were dry etched through an ICP-RIE system. We show that with optimal power Si nanocones can be produced that act as BSi with very low reflectance. ICP power of the ICP-RIE strongly affects the etching rate and selectivity. At an ICP power of 100 W, the etching selectivity is high, but the etching rate is very low, leading to the incomplete formation of Si nanopillars with an average height of 150 nm and low aspect ratio, as shown in Figure 1a. Increasing ICP power to 125 W results in a compromise between substrate selectivity and etching rate, providing Si nanopillars with more height (250 nm) and an enhanced aspect ratio (Figure 1 b). As observed in Figure 1c, the etching depth reaches its maximum at an ICP power of 150 W, providing a conelike, vertically aligned, and well-separated Si nanopillar array of height 400 nm on the substrate surface. Figure 1d illustrates that the Si nanopillars are etched out under a further increase in ICP power (200 W) because of low etching selectivity and a high etching rate. Figure 1e shows a high-resolution image of the Si nanopillars fabricated with ICP power of 150 W. For comparison, the micrograph of MACE fabricated conelike Si nanopillars is presented in Figure 1f. There are several reports available in the literature for growing antireflecting Si surfaces using solution-based chemical technique also. However, a comparison of performance of the device fabricated on Si nanostructures prepared by solution- and plasma-based techniques is essential. In this regard, conelike Si nanostructures have also been fabricated using MACE. Figure 1e,f shows the magnified images of Si nanostructures grown by ICP-RIE technique using 150 W ICP power and a solution method. FESEM micrographs clearly reveal that the surface of ICP-RIE-grown nanostructure is very smooth and defect free. On the other hand, MACE-grown nanostructures have relatively rough surface. The above observations are corroborated by the transmission electron microscopy (TEM) images of a single Si nanocone presented in the insets of Figure 1e,f for ICP-RIE- and MACE-grown samples, respectively.

Figure 2 shows the optical reflectance spectra of Si nanostructured samples grown at different ICP powers (P).

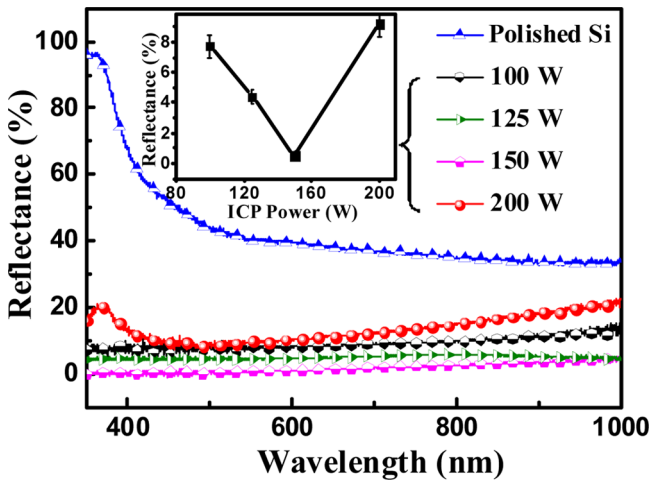

Figure 2. Reflectance spectra of polished Si surface and Si nanostructures fabricated through ICP-RIE technique at different ICP powers. Inset shows the variation of reflectance R with plasma power (P) at $\lambda \approx$ 500−550 nm.

All nanopillar samples exhibit much lower reflectance in UV−visible wavelength range in comparison to bulk Si wafer. Average reflectances (R) of Si nanostructured samples grown at P = 100, 125, 150, and 200 W are found to be 12, 6, 1.8, and 16%, respectively, in 350−1000 nm wavelength range. In the inset of Figure 2, we show the variation of R as a function of P for $\lambda \approx$ 500−550 nm, the maxima of the solar spectra. This excellent antireflection property arises because the vertical Si nanostructure acts as a subwavelength-structured surface. Such a textured surface on Si provides an effective medium with a smooth transition of the refractive index from air to Si because the fractional area occupied by Si as a function of the depth across the textured layer increases progressively. This is established through modeling and simulation results described in the next subsection. The observed average reflectance of ~2.0% for samples grown at 150 W seems to be very promising for solar cell applications and motivated us to fabricate a heterojunction solar cell on this sample.

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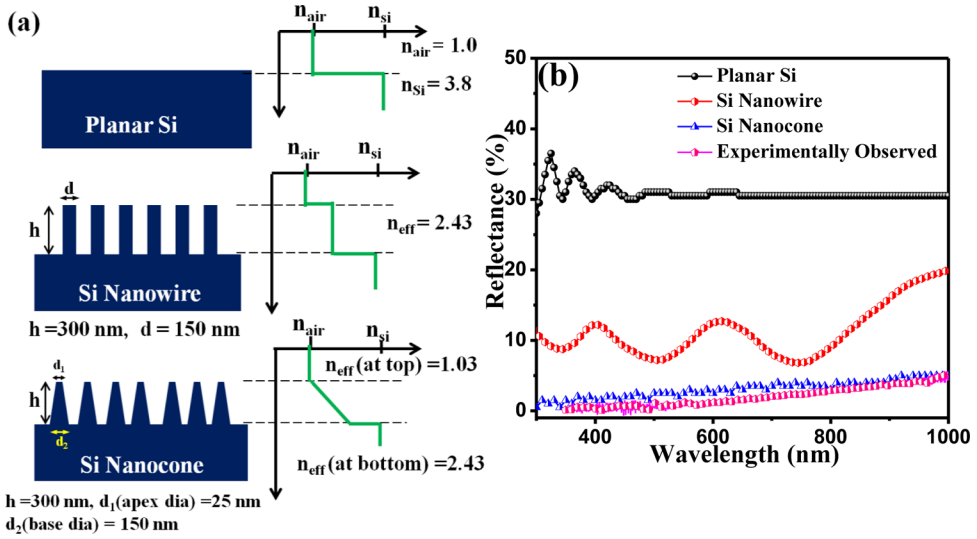

Figure 3. (a) Schematic illustrations of planar Si, Si nanowire, and Si nanocone and their corresponding effective refractive index profiles across air-to-Si wafer, air-to-Si nanorod, and air-to-Si nanocone, respectively. (b) Calculated reflectance spectra of planar Si, Si nanorods, and Si nanocones arrays. Experimentally measured reflectance data for the BSi fabricated at 150 W ICP power is also presented for comparison.

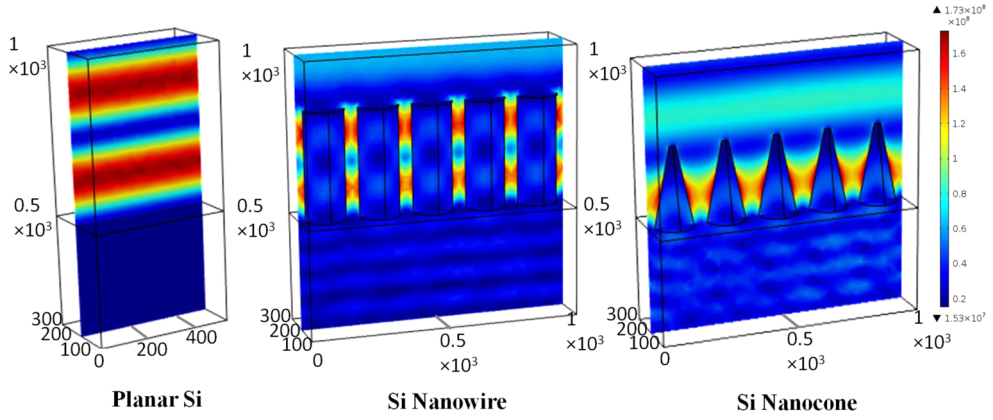

Figure 4. Electric field distribution ($|E|^2$) in planar Si (left), Si nanorods (middle), and Si nanocone arrays (right) under 600 nm incident light.

3.2. Simulation of Reflectance. The optical properties of vertically oriented Si nanowire and nanocone arrays in visible to near-IR region were studied by simulation and modeling. To test the effect of nanostructure geometry on optical properties, such as reflectance and field distribution, we considered two different nanostructures: nanowire array and nanocone array. The bulk planar Si is also included for comparison. The light-trapping scheme and field intensity variation of Si nanostructures is solved by a numerical model based on Fresnel's equation using the RF module of Comsol multiphysics (4.4) software. The geometry of the modeled structures is shown in Figure 3a. For calculation, the dimension of Si nanocone array has been chosen as the average for the highest aspect ratio Si nanocones fabricated at 150 W ICP power (shown in Figure 1e). The nanocone array has a base diameter of 150 nm, an apex diameter of 25 nm, a period of 200 nm, and a height of 300 nm. For the nanorod array, period and height are chosen as the same as those of the nanocone one, whereas the uniform rod diameter is taken as the base diameter of the nanocone (150 nm). The incident direction of light is chosen at an angle of 10° to the surface normal. The effective refractive index (n_{eff}) gradient of the nanocone and nanorod arrays has been estimated by the relation[26]

$$n_{eff}(h) = \{f(h)\, n^q_{Si} + [1 - f(h)] n^q_{air}{}^{1/q}\} \quad (1)$$

which is derived from the effective medium approximation (EMA) theorem, where n_{Si} and n_{air} are, respectively, the refractive indices of Si and air, q the exponent is $^2/_3$, and $f(h)$ is the fill factor, which is calculated from the areal ratio of nanostructure surface to the total surface at a particular height (h).

The schematic diagram and the corresponding refractive index profiles of the nanostructures are presented in Figure 3a. For the cone, at the top surface the $n_{eff} \approx 1.03$. This is close to n_{air}. The value of n_{eff} varies smoothly as shown in the graph, and at the base of the cone, it reaches a value of ~2.43. The gradient in n_{eff} will be shown to play an important role to suppress the resultant reflectance. For the nanorod, $n_{eff} \approx 2.43$ throughout the height of the nanorod array. This leads to two steps in refractive index, one at the top ($\Delta n_{top} = n_{eff} - n_{air} = 1.43$) and another at bottom ($\Delta n_{bottom} = n_{Si} - n_{eff} = 1.37$), which are responsible for enhanced reflectance in the nanorod array.

Figure 3b shows the simulated results of reflectance spectra over a wavelength range of 200−1000 nm for planar Si, Si nanorod arrays, and Si nanocone arrays. The calculated value of average reflectance for planar Si, Si nanorod, and Si nanocone arrays have been found to be 30, 11, and 2.5%, respectively. In

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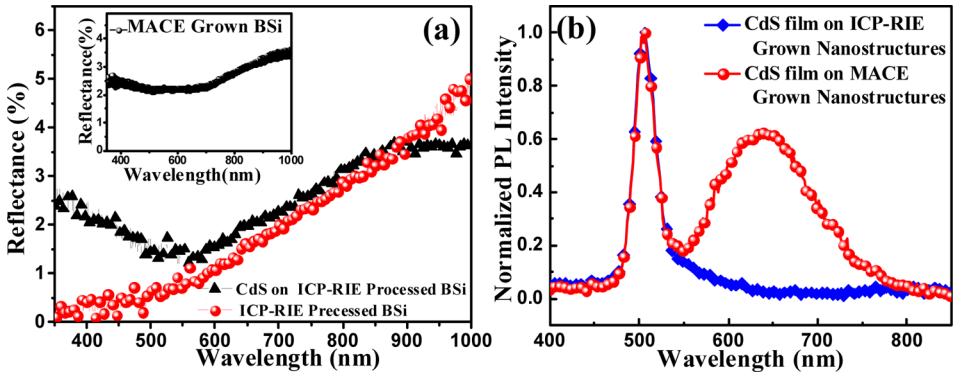

Figure 5. (a) Reflectance spectrum of CdS/Si heterojunction on ICP-RIE-grown Si nanostructures along with the reflectance spectrum of the ICP-RIE-processed BSi. Inset shows the reflectance spectrum of MACE-grown BSi. (b) Normalized photoluminescence spectra of CdS/Si heterojunction fabricated on ICP-RIE- and MACE-grown Si nanostructures.

the same graph, we show the observed reflectance spectra for the nanocone array fabricated at an ICP power 150 W. The calculated reflectance values for nanocone structures are in excellent agreement with the experimentally observed ones. The results show a significant decrease in the reflectance for nanocone geometry compared to those of the nanorod structure and planar Si. The experimentally observed reflectivity is slightly less than that of the calculated one which may be due to the deviation of geometrical dimension from the average and the difference of doping level considered for calculation. Recently, Yung et al.[27] and Wang et al.[28] have also shown that the randomness in geometrical dimensions further reduces the reflectivity.

To verify the light trapping location within different nanostructures, the cross-sectional electric field intensity distribution ($|E|^2$) have been simulated at a wavelength of 600 nm for planar Si, Si nanorods, and Si nanocone arrays. We have considered that an incident electromagnetic (EM) wave propagates downward as plane waves from the top to the bottom of each nanostructure. Figure 4 compares the field distribution within each nanostructure with a color index. The field distribution for planar Si showed ordered reflected wavetrains with matching amplitudes (color coded), which will interfere to result in fringing. In the case of the Si nanorod sample, the electric fields are located along the sidewall surface, where light trapping occurs. The reflected wavetrains in nanorod structure exhibit a fringing pattern similar to that in planar Si. The noticeable difference in the field distribution for nanocone geometry in comparison to nanorod and planar geometry is the absence of fringing patterns, indicating that the interference is not so pronounced because of extremely weak reflected wavetrains for this geometry.

3.3. Optical Characteristics of n-CdS on p-Si Nanocones. The radial heterojunction solar cells were fabricated by depositing ∼50 nm thick CdS films on both ICP-RIE- and MACE-grown Si nanostructures (as well as on planar Si), keeping all the experimental condition same for all the devices. To show that deposition of CdS does not change the reflectance, the data for bare nanocone as well as that of the CdS-coated BSi are presented in Figure 5a. The data clearly indicate that even after CdS deposition the heterostructure maintains the antireflecting feature of BSi (average reflectance ∼2%). The observed dip in the reflectance spectra around 500 nm may originate from the absorption of the CdS film around its band gap energy. For comparison, in the inset of Figure 5a we also show the reflectance for the MACE-grown nanostructures. The average reflectance for chemically grown nanostructures (∼2%) is also comparable to that of the ICP-RIE-grown BSi.

To assess the quality of the nanostructures, we have recorded the photoluminescence (PL) spectra. It is expected that the presence of defective nanostructure, if any, will give rise to a PL signal for defect-related emission in addition to what is expected from the near-band-edge (NBE) emission. Figure 5b presents the normalized spectra recorded at room temperature for CdS/Si heterostructures fabricated on both ICP-RIE- and MACE-grown Si nanostructures. Under excitation by a 325 nm pump, the PL emission of CdS/Si heterojunction on ICP-RIE-processed nanostructure is found to be narrow and centered around 505 nm. This emission is attributed to the NBE peak of CdS.[22] The PL spectrum of CdS/Si heterojunction fabricated on MACE-grown Si nanostructures exhibits an additional broad emission peak centered around 640 nm along with the NBE emission (505 nm) of CdS. The observed PL band around 640 nm is attributed to the porous nature of the nanostructured Si surface.[29] The absence of PL emission at 640 nm from CdS/Si heterojunction further confirms the formation of very smooth surface in ICP-RIE-processed nanostructure.

3.4. Dark *I*–*V* Characteristics of n-CdS/p-Si Heterojunction Cells. Because deposited CdS exhibits n-type conductivity with a doping concentration of $\sim 10^{14}/cm^3$,[22] the deposition of CdS on vertically oriented Si (p-type) nanostructures leads to the formation of a core–shell-type radial heterojunction. To compare the electrical transport and solar cell characteristics of a CdS/Si nanoheterojunction with those of the planar one, a planar thin-film heterojunction has also been fabricated. The room-temperature dark current–voltage (I–V) characteristics of fabricated Si/CdS core–shell and planar heterojunctions is shown in Figure 6. The extracted data are summarized in Table 1. The inset of this figure shows the schematic diagram of the devices fabricated on vertically oriented Si nanostructures. The forward current of the CdS/Si heterojunction fabricated on ICP-RIE-processed BSi reaches around 10 mA at a bias of 1 V, whereas it is much lower in cells fabricated on both MACE-grown nanostructures and planar Si. However, the reverse saturation current (measured at −1 V) is ≈3 μA in the heterojunction, with BSi showing a rectification ratio approaching 3×10^3. The reverse saturation current in the other devices is much larger, leading to a low rectification ratio (Table 1). The observed high forward current in the radial heterojunction solar cell fabricated on ICP-RIE-grown BSi

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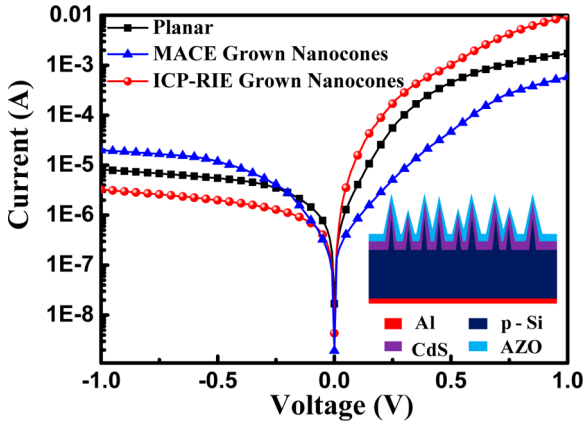

Figure 6. Dark current−voltage (I−V) characteristics of fabricated Si/CdS heterojunction on ICP-RIE- and MACE-grown nanostructure and planar heterojunctions at room temperature. Inset shows the schematic diagram of the devices fabricated on vertically oriented Si nanostructures.

results from its small R_S value due to a very large specific surface area of Si nanostructures.

The dark I−V characteristics are fitted with the diode equation $I = I_0 \exp(eV/nk_BT)$ for small positive voltage, where I_0 is the dark saturation current, n is the ideality factor, and k_B is the Boltzmann constant. The diode ideality factor for solar cell fabricated on ICP-RIE ≈ 2.6 is found to be much lower compared to those of cells fabricated on MACE-grown nanostructures and planar Si (Table 1). The relatively higher reverse current in junctions fabricated on MACE-grown Si nanostructures, in comparison to those fabricated on ICP-RIE-grown nanostructures and planar Si, is mainly due to the presence of a high density of the interface states in chemically etched samples. The above diode characteristics extracted using dark current analysis signify that the rectification behavior for the junction fabricated on ICP-RIE-grown nanostructure is much superior to that of junctions fabricated on solution-grown nanostructure and planar Si. This corroborates the inference reached from the PL results presented in Figure 5b.

3.5. Characteristics of n-CdS/p-Si Heterojunction Cells Under Illumination. The current density−voltage (J−V) characteristics of fabricated solar cell devices have been measured under 100 mW/cm^2 with AM 1.5 simulated solar irradiation condition. The data for all the cells are presented in Figure 7a. ICP-RIE-grown BSi exhibits a short-circuit current density (J_{sc}) of 16.5 mA/cm^2, an open circuit voltage (V_{oc}) of 0.43 V, and fill factor (FF) of 41.9%, resulting in an efficiency of 2.96%. In comparison, the MACE-grown nanostructures show J_{sc} = 4.75 mA/cm^2, V_{oc} = 0.42 V, and FF = 33.1%, leading to an efficiency of 0.66%. The corresponding values for the solar cell fabricated on planar Si are 1.43 mA/cm^2, 0.43 V, and 22.8 and 0.15%, respectively. The photovoltaic parameters of three devices are listed in Table 2.

The power conversion effiency of solar cells fabricated on textured Si fabricated through ICP-RIE and MACE has been found to be much higher than that of the planar control device (∼0.15%). A larger interfacial area and excellent antireflection property leads to higher efficiency for both nanotextured devices. The device fabricated on ICP-RIE-grown nanostructures shows a promising efficiency of 2.96%, which is nearly five times higher than that obtained for the MACE-grown nanostructure device (0.66%). Despite having nearly equal average reflectance and same aspect ratio, devices fabricated on ICP-RIE-grown nanostructure templates exhibit much better efficiency, indicating the importance of the defect-free surfaces in the plasma-processed nanostructure. It should be noted that the surfaces of MACE-grown nanostructures are rough, having a large number of surface states leading to large interface state density. These surface states lead to large and broad PL centered around 650 nm and high ideality factor of the heterojunction, which results in poor power conversion efficiency.

Figure 7b shows the measured EQE of photovoltaic devices fabricated on Si nanostructure templates grown via MACE and ICP-RIE and on planar Si. All three samples show broad spectral response (400−1200 nm) arising from absorption of CdS film and the Si underneath. Photocurrent contribution due to NBE absorption form CdS film (∼510 nm) is clearly observed for all three devices. The absorption from the porous surface of Si nanostructure (600−750 nm) for the solar cell fabricated on MACE-grown nanostructure is also evident. A peak EQE of ∼65% for the ICP-RIE-grown BSi device reveals the efficient carrier extraction and collection for the device. The solar cell fabricated on MACE-grown nanocones shows a peak EQE of only ∼20%. The recombination of photogenerated carriers at interface defect states could be responsible for poor EQE in MACE-based devices.

The fabrication process of BSi controls the structural and surface quality. The structural and surface quality of the semiconductor nanostructures is an important factor that determines the minority carrier lifetime and surface recombination velocity. These in turn affect the performance of photovoltaic devices. To investigate the effect of BSi fabrication technique on solar cell performance, we have extracted the minority carrier lifetime using open-circuit photovoltage (V_{oc}) decay measurements.[30−32] The recombination-limited effective minority carrier lifetime is related to the initial slope (dV_{oc}/dt) of the decay edge by the relation[30]

$$\tau = -\frac{kT}{q}\frac{2}{\left(\frac{dV_{oc}}{dt}\right)} \quad (2)$$

where τ is the effective minority carrier lifetime, k is the Boltzmann constant, q is the elementary charge, and T is the operating temperature of the device. Figure 8 shows the typical photovoltage decay characteristics for solar cells fabricated using differently made BSi, recorded at the trailing edge of 980 nm laser source pulse with an illuminated power of 28 mW cm^{-2}. The open-circuit voltage decay profiles reveal that the recombination rate in a device fabricated on MACE-grown Si

Table 1. Dark Characteristics of Devices Fabricated on ICP-RIE- and MACE-Grown Nanostructure and Planar Si

device	I(forward) V = 1 V (mA)	I(reverse) V = −1 V (μA)	ideality factor (n)	rectification ratio
planar	1.7 ± 0.10	8.2 ± 0.4	3.4 ± 0.2	209 ± 7
MACE-grown nanocones	0.5 ± 0.06	20.3 ± 1.2	7.2 ± 0.3	33 ± 2
ICP-RIE-grown nanocones	10.1 ± 0.80	3.0 ± 0.2	2.6 ± 0.2	2968 ± 95

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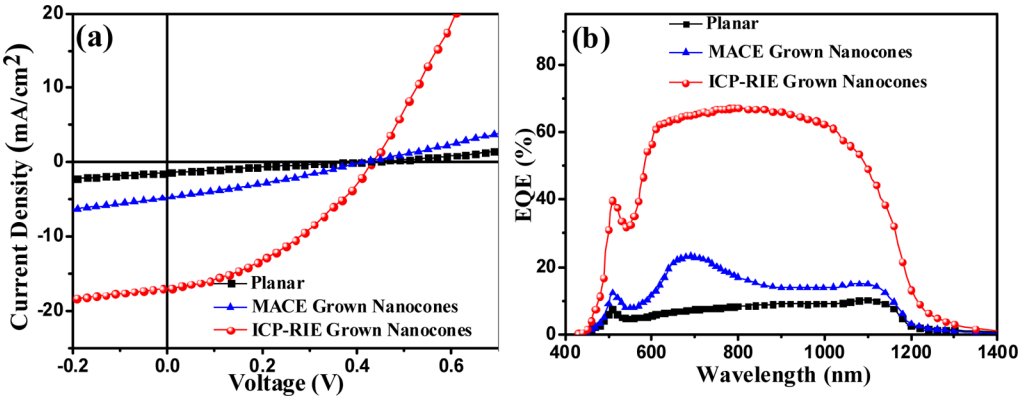

Figure 7. (a) $J-V$ characteristics of solar cell devices fabricated on ICP-RIE- and MACE-grown nanostructure and planar Si under 100 mW/cm^2 AM 1.5 simulated solar irradiation condition. (b) External quantum efficiency (EQE) of solar cell devices fabricated on Si nanostructure templates grown via ICP-RIE and MACE and on planar Si.

Table 2. Photovoltaic Characteristics of Devices Fabricated on ICP-RIE- and MACE-Grown Nanostructure and Planar Si under 100 mW/cm^2 (AM 1.5) Simulated Solar Irradiation Condition

device	J_{sc} (mA/cm^2)	V_{oc} (V)	FF (%)	η (%)
planar	1.56 ± 0.13	0.43 ± 0.05	22.8 ± 3	0.15 ± 0.01
MACE-grown nanocones	4.75 ± 0.34	0.42 ± 0.05	33.1 ± 2	0.66 ± 0.04
ICP-RIE-grown nanocones	16.5 ± 0.82	0.43 ± 0.05	41.9 ± 2	2.96 ± 0.21

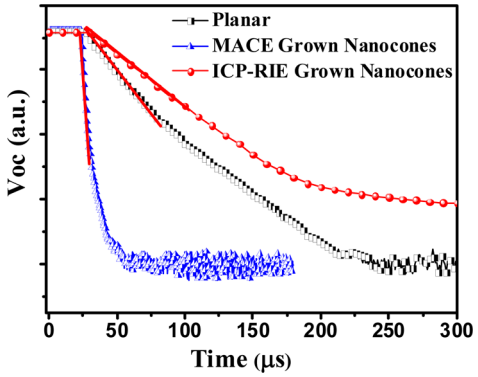

Figure 8. Photoinduced V_{oc} decay profile for solar cells fabricated on ICP-RIE- and MACE-grown nanostructure along with those fabricated with planar Si. Red line at the initial portion of decay profile represents the best linear fit to determine the initial slope for the calculation of recombination-limited carrier lifetime.

nanocones is much higher in comparison to that of devices fabricated on ICP-RIE-grown BSi and planar Si. The calculated minority carrier lifetime using the initial slope of the V_{oc} decay curve is found to be ∼4.6, 68.6, and 57.2 μs for solar cells fabricated on MACE-grown and ICP-RIE-processed BSi and planar Si, respectively, The presence of a large defect density on the porous surface of MACE-grown Si nanocones leads to the enhanced surface recombination rates, resulting in a carrier lifetime that is at least one order less than that seen in the devices based on ICP-RIE-processed BSi and planar Si. The minority carrier lifetime is of similar order in the later samples.

Generally, the effective minority carrier lifetime in a silicon-based solar cell depends on the surface and bulk recombination rates. The measured effective carrier lifetime (τ_{meas}) in terms of bulk (τ_{bulk}) and surface recombination rates is expressed as[33,34]

$$\frac{1}{\tau_{meas}} = \frac{1}{\tau_{bulk}} + \frac{S_1 + S_2}{W} \quad (3)$$

where S_1 and S_2 are the recombination velocity at the front and back surfaces, respectively, and W is the sample width. Because the bottom Si surface is unaffected in ICP-RIE- or MACE-processed BSi, S_2 is negligibly small in comparison to S_1. However, their values are comparable in the case of planar Si. With the assumption of dominant recombination at the front surface for BSi and comparable magnitude for planar Si, the above equation can be written as

$$\frac{1}{\tau_{meas}} \approx \frac{1}{\tau_{bulk}} + \frac{S_1}{W} \quad (4)$$

for black Si and

$$\frac{1}{\tau_{meas}} \approx \frac{1}{\tau_{bulk}} + \frac{2S_1}{W} \quad (5)$$

for planar Si.

In our case, all Si/CdS heterojunction solar cell devices have been fabricated on 400 μm thick (W = 400 μm) CZ p-Si wafers with a nominal doping concentration of ∼6 × 10^{15} cm^{-3}. Using the bulk minority carrier lifetime of Si for the above doping level, the surface recombination velocity of nanocone surface (Si/CdS interface) for BSi grown via MACE and ICP-RIE processes has been calculated to be 86.0 and 5.8 m/sec, respectively. In comparison, the surface recombination velocity for planar Si is found to be 3.5 m/sec. The result indicates that the MACE-gown Si nanocone suffers from severe surface degradation in comparison to the surface of the others. Though the surface recombination velocity of ICP-RIE-processed sample is higher than that of the planar one, a higher minority carrier lifetime and a lower ideality factor of the Si/CdS heterojunction for the former results in improved photovoltaic performance. The extracted values of minority carrier lifetime and surface recombination velocity for the heterojunctions fabricated on various Si surfaces are in good agreement with the observed photovoltaic parameters, which further indicates that the low surface damage during the fabrication process is highly desirable for BSi solar cells. It may be noted that the grown

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CdS film in the PLD process is not perfectly epitaxial but highly oriented leading to higher idealty factors of CdS/Si heterojunction diodes. Therefore, the optimization of contact formation and a suitable epitaxial growth process for CdS would lead to the further enhancement of solar cell device performance.

4. CONCLUSIONS

We have synthesized highly antireflective, vertically aligned Si nanostructures (BSi) on p-Si wafers using a ICP-RIE technique. The as-fabricated Si nanostructures exhibit very low reflectivity (~2% in the wavelength range 350−1000 nm) under an optimized etching conditions. Through simulations, we conclude that the reflectivity reaches a low value because the effective refractive index (n_{eff}) varies smoothly from the value for the air at the top surface (where light falls) to that of Si at the base at the wafer. To establish the enabling role of BSi on solar cell efficiency, we fabricated n-CdS/p-Si heterojunction solar cells on ICP-RIE nanostructures. Such a cell reaches a power conversion efficiency of ~3% with 1.5AM illumination. For comparison, similar cells fabricated on MACE-fabricated nanostructure and planar Si show much lower efficiencies (~0.66 and 0.15%, respectively). The minority carrier lifetime for planar Si and MACE- and ICP-RIE-grown BSi extracted using transient photovoltage characteristics is found to be as 57.2, 68.6, and 4.6 μs, respectively. The large defect density at the rough surface of MACE-grown Si nanocones resulted in very high surface recombination velocity and diode idealty factor. The investigation was done with a specific type of solar cell to establish the value addition of ICP-RIE plasma-processed BSi, leading to enhanced efficiency. However, it is a generic observation, and this may act as an efficiency enhancer in other types of Si-based solar cells as well.

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Notes

The authors declare no competing financial interest.

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REFERENCES

(1) Tian, B.; Zheng, X.; Kempa, T. J.; Fang, Y.; Yu, N.; Yu, G.; Huang, J.; Lieber, C. M. Coaxial Silicon Nanowires as Solar Cells and Nanoelectronic Power Sources. *Nature* **2007**, *449*, 885−889.

(2) Wang, X.; Peng, K. Q.; Pan, X. J.; Chen, X.; Yang, Y.; Li, L.; Meng, X. M.; Zhang, W. J.; Lee, S. T. High-Performance Silicon Nanowire Array Photoelectrochemical Solar Cells through Surface Passivation and Modification. *Angew. Chem., Int. Ed.* **2011**, *50*, 9861−9865.

(3) Katiyar, A. K.; Sinha, A. K.; Manna, S.; Ray, S. K. Fabrication of Si/ZnS Radial Nanowire Heterojunction Arrays for White Light Emitting Devices on Si Substrates. *ACS Appl. Mater. Interfaces* **2014**, *6*, 15007−15014.

(4) Oh, J.; Yuan, H. C.; Branz, H. M. An 18.2%-Efficient Black-Silicon Solar Cell Achieved Through Control of Carrier Recombination in Nanostructures. *Nat. Nanotechnol.* **2012**, *7*, 743−748.

(5) Savin, H.; Repo, P.; von Gastrow, G.; Ortega, P.; Calle, E.; Garín, M.; Alcubilla, R. Black Silicon Solar Cells With Interdigitated Back-Contacts Achieve 22.1% Efficiency. *Nat. Nanotechnol.* **2015**, *10*, 624−628.

(6) Koynov, S.; Brandt, M. S.; Stutzmann, M. Black Nonreflecting Silicon Surfaces for Solar Cells. *Appl. Phys. Lett.* **2006**, *88*, 203107.

(7) Linnros, J.; Lalic, N. High Quantum Efficiency For a Porous Silicon Light Emitting Diode Under Pulsed Operation. *Appl. Phys. Lett.* **1995**, *66*, 3048−3050.

(8) Lalic, N.; Linnros, J. Characterization of a Porous Silicon Diode With Efficient and Tunable Electroluminescence. *J. Appl. Phys.* **1996**, *80*, 5971−5977.

(9) Ivanova, E. P.; Hasan, J.; Webb, H. K.; Gervinskas, G.; Juodkazis, S.; Truong, V. K.; Wu, A. H. F.; Lamb, R. N.; Baulin, V. A.; Watson, G. S.; Watson, J. A.; Mainwaring, D. E.; Crawford, R. J. Bactericidal Activity of Black Silicon. *Nat. Commun.* **2013**, *4*, 2838.

(10) Rong, J.; Masarapu, C.; Ni, J.; Zhang, Z.; Wei, B. Tandem Structure of Porous Silicon Film on Single-Walled Carbon Nanotube Macrofilms for Lithium-Ion Battery Applications. *ACS Nano* **2010**, *4*, 4683−4690.

(11) Abdolahad, M.; Shashaani, H.; Janmaleki, M.; Mohajerzadeh, S. Silicon Nanograss Based Impedance Biosensor for Label free Detection of Rare Metastatic Cells Among Primary Cancerous Colon Cells, Suitable for More Accurate Cancer Staging. *Biosens. Bioelectron.* **2014**, *59*, 151−159.

(12) Schmidt, M. S.; Hübner, J.; Boisen, A. Large Area Fabrication of Leaning Silicon Nanopillars for Surface Enhanced Raman Spectroscopy. *Adv. Mater.* **2012**, *24*, OP11−OP18.

(13) Sainiemi, L.; Jokinen, V.; Shah, A.; Shpak, M.; Aura, S.; Suvanto, P.; Franssila, S. Non-Reflecting Silicon and Polymer Surfaces by Plasma Etching and Replication. *Adv. Mater.* **2011**, *23*, 122−126.

(14) Dussart, R.; Tillocher, T.; Lefaucheux, P.; Boufnichel, M. Plasma Cryogenic Etching of Silicon: from the Early Days to Today's Advanced Technologies. *J. Phys. D: Appl. Phys.* **2014**, *47*, 123001.

(15) Kabashin, A. V.; Delaporte, P.; Pereira, A.; Grojo, D.; Torres, R.; Sarnet, T.; Sentis, M. Nano Fabrication With Pulsed Lasers. *Nanoscale Res. Lett.* **2010**, *5*, 454−463.

(16) Li, Y.; Zhang, J.; Zhu, S.; Dong, H.; Wang, Z.; Sun, Z.; Guo, J.; Yang, B. Bioinspired Silicon Hollow-Tip Arrays for High Performance Broadband Anti-Reflective and Water-Repellent Coatings. *J. Mater. Chem.* **2009**, *19*, 1806−1810.

(17) Srivastava, S. K.; Kumar, D.; Vandana; Sharma, M.; Kumar, R.; Singh, P. K. Silver Catalyzed Nano-Texturing of Silicon Surfaces for Solar Cell Applications. *Sol. Energy Mater. Sol. Cells* **2012**, *100*, 33−38.

(18) Kleimann, P.; Linnros, J.; Juhasz, R. Formation of Three-Dimensional Microstructures by Electrochemical Etching of Silicon. *Appl. Phys. Lett.* **2001**, *79*, 1727−1729.

(19) Katiyar, A. K.; Sinha, A. K.; Manna, S.; Aluguri, R.; Ray, S. K. Optical Photoresponse of CuS−n-Si Radial Heterojunction with Si Nanocone Arrays Fabricated by Chemical Etching. *Phys. Chem. Chem. Phys.* **2013**, *15*, 20887−20893.

(20) Wenas, W. W.; Riyadi, S. Carrier Transport in High-Efficiency ZnO/SiO2/Si Solar Cells. *Sol. Energy Mater. Sol. Cells* **2006**, *90*, 3261−3267.

(21) Hayden, O.; Greytak, A. B.; Bell, D. C. Core−Shell Nanowire Light-Emitting Diodes. *Adv. Mater.* **2005**, *17*, 701−704.

(22) Manna, S.; Das, S.; Mondal, S. P.; Singha, R.; Ray, S. K. High Efficiency Si/CdS Radial Nanowire Heterojunction Photodetectors Using Etched Si Nanowire Templates. *J. Phys. Chem. C* **2012**, *116*, 7126−7133.

(23) Coluzza, C.; Garozzo, M.; Maletta, G.; Margadonna, D.; Tomaciello, R.; Migliorato, P. nCdS/pSi Heterojunction Solar Cells. *Appl. Phys. Lett.* **1980**, *37*, 569−572.

(24) García, F. J.; Ortíz-Conde, O.; Sa-Neto, A. CdS/pSi Solar Cells Made by Serigraphy. *Appl. Phys. Lett.* **1988**, *52*, 1261−1263.

DOI: 10.1021/acsami.5b04978
ACS Appl. Mater. Interfaces 2015, 7, 23445−23453

(25) He, C.; Han, C. B.; Xu, Y. R.; Li, X. J. Photovoltaic Effect of CdS/Si Nanoheterojunction Array. *J. Appl. Phys.* **2011**, *110*, 094316.
(26) Stavenga, D. G.; Foletti, S.; Palasantzas, G.; Arikawa, K. Light on the Moth-Eye Corneal Nipple Array of Butterflies. *Proc. R. Soc. London, Ser. B* **2006**, *273*, 661−667.
(27) Hung, Y. J.; Lee, S. L.; Wu, K. C.; Tai, Y.; Pan, Y. T. Antireflective Silicon Surface with Vertical Aligned Silicon Nanowires Realized by Simple Wet Chemical Etching Processes. *Opt. Express* **2011**, *19*, 15792−15802.
(28) Wang, Z. Y.; Zhang, R. J.; Wang, S. Y.; Lu, M.; Chen, X.; Zheng, Y. X.; Chen, L. Y.; Ye, Z.; Wang, C. Z.; Ho, K. M. Broadband Optical Absorption by Tunable Mie Resonances in Silicon Nanocone Arrays. *Sci. Rep.* **2015**, *5*, 7810.
(29) Qu, Y.; Liao, L.; Li, Y.; Zhang, H.; Huang, Y.; Duan, X. Electrically Conductive and Optically Active Porous Silicon Nanowires. *Nano Lett.* **2009**, *9*, 4539−4543.
(30) Johnston, W. K.; Pattantyus-Abraham, A. G.; Clifford, P. J.; Myrskog, H. S.; Hoogland, S.; Shukla, H.; Klem, J. D. E.; Levina, L.; Sargent, H. E. Efficient Schottky-Quantum-Dot Photovoltaics: The Roles of Depletion, Drift, and Diffusion. *Appl. Phys. Lett.* **2008**, *92*, 122111−3.
(31) Rath, K. A.; Bernechea, M.; Martinez, L.; de Arquer, F. P. G.; Osmond, J.; Konstantatos, G. Solution-Processed Inorganic Bulk Nano-Heterojunctions and Their Application to Solar Cells. *Nat. Photonics* **2012**, *6*, 529−534.
(32) Mahan, J. E.; Ekstedt, T. W.; Frank, R. I.; Kaplow, R. Measurement of Minority Carrier Lifetime in Solar Cells from Photo-Induced Open-circuit Voltage Decay. *IEEE Trans. Electron Devices* **1979**, *26* (5), 733−739.
(33) Yu, P.; Tsai, C. Y.; Chang, J. K.; Lai, C. C.; Chen, P. H.; Lai, Y. C.; Tsai, P. T.; Li, M. C.; Pan, H. T.; Huang, Y. Y.; Wu, C. I.; Chueh, Y. L.; Chen, S. W.; Du, C. H.; Horng, S. F.; Meng, H. F. 13% Efficiency Hybrid Organic/Silicon- Nanowire Heterojunction Solar Cell via Interface Engineering. *ACS Nano* **2013**, *7* (12), 10780−10787.
(34) Nam, D.; Kang, J. H.; Brongersma, M. L.; Saraswat, K. C. Observation of Improved Minority Carrier Lifetimes in High-Quality Ge-on-Insulator Using Time-Resolved Photoluminescence. *Opt. Lett.* **2014**, *39* (21), 6205−6208.

DOI: 10.1021/acsami.5b04978
ACS Appl. Mater. Interfaces 2015, 7, 23445−23453